Remarks

Thorough examination by the Examiner is noted and appreciated.

The Specification haa been amended to correct grammatical errors.

The claims have been amended and new claims added to clarify Applicants invention.

Support for the amendments is found in the original claims and in the Specification. No new matter has been added.

For example support for the amendments is found in the Figures and in the Specification at paragraph 0022 of the Specification:

"Referring to Figure 1E, in a **critical** aspect of the invention, a wet or dry etching process is then carried out to remove a portion of the nitride spacer 18B, to form a **Slim (reduced width) oxide/nitride spacer width from W2 to W1.** Advantageously, in the spacer thinning process a portion of the underlying SDE region e.g., 20A is exposed by the reduced width amount e.g., W3. For example, a maximum width W1 of the Slim spacers is preferably less than a width W2 of the SDE doped regions e.g., 20A measured to an edge of the S/D doped region 22A.

It will be appreciated that the desired reduction in width of the nitride spacer portion 18B will vary depending on the gate length and the oxide/nitride spacer width W2 present for the S/D implant process prior to thinning, a desired reduction in S/D resistance, and a desired increase in channel stress. Preferably, however, the Slim width W1 of the oxide/nitride spacer 18A and 18B measured from the polysilicon or metal gate electrode sidewall 14, is reduced by greater than about 20 percent of W2 to achieve a desired electrical resistance decrease in S/D region e.g., 22A and SDE region e.g., 20A and/or an increase in channel stress in channel region e.g., 26. In an exemplary embodiment, for a CMOS gate structure having a gate length (L_G), of about 400 Angstroms and a pre-Slim spacer width W2 of about 650 Angstroms, the spacer is reduced to a width W1 of less than about 500 Angstroms, more preferably less than about 350 Angstroms."

Drawing Objections

Paragraph 0020 has been amended to overcome Examiners objections to the Drawings.

Claim Rejections under 35 USC 112

Claim 4 has been amended to overcome Examiners rejection.

Claim Rejections under 35 USC 102

1. Claim 1 stands rejected under 35 USC 102(b) as being anticipated by Miyanaga (JP 11-233769 or US 6,897,526).

Note col and line number references are made to the US patent.

Miyanaga disclose a method for forming a punch through stopper under a gate electrode by introducing impurities into the substrate along the <110> axis and underlying the gate electrode (see Abstract). Miyanaga discloses that the <100> axis direction agrees with the direction connecting the source and drain. Miyanaga also **discloses conventional spacers** overlying the SDE (LDD) region (see Figure 9).

Miyanaga discloses forming oxide spacers (item 417) by etchback following formation of an LDD region (SDE region) (see Figure 5B) adjacent the gate structure where the spacers are then used as a mask in forming the source and drain regions at a higher doping (see Figure 6A) and where the entire LDD region (SDE region) underlies

the oxide spacers (see e.g., col 8, lines 45-67).

Thus, Miyanaga fails to disclose several aspects of Applicants disclosed and claimed invention including **slim (thinned) spacers** as claimed by Applicant and as further defined in the Specification at paragraph 0022, and is clearly insufficient to anticipate Applicants disclosed and claimed invention.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

2. Claims 21, 24, and 28-30 stand rejected under 35 USC 102(b) as being anticipated by Huang (US 6,140,192).

Huang et al. disclose a method for forming thinned spacers where the LDD (SDE) regions are formed prior to thinning the spacer and where portions of the underlying SDE (LDD) region are exposed (see Figure 4D; col 6, lines 11 - 38). The thinned spacers of Huang are formed having **a top portion lower than the top portion of the gate**

electrode (see Figure 4E), prior to **forming a metal layer over the gate structure in a salicide formation process** (see col 6, lines 11-24 col 6, lines 38-47).

Thus, Huang et al. do not disclose several aspects of Applicants disclosed and claimed invention including:

"wherein said thinned spacers have a top portion at about the same level as the top portion of the gate electrode"

and

"at least one stressed dielectric layer disposed overlying the gate structure including said thinned spacers to exert a stress through said thinned spacers on said channel region."

Thus, Huang fails to disclose several aspects of Applicants disclosed and claimed invention and is clearly insufficient to anticipate Applicants disclosed and claimed invention.

Claim Rejections under 35 USC 103

3. Claim 2 stands rejected under 35 USC 103(a) as being unpatentable over Miyanaga, above, in view of Cabral (US 6927117).

Applicants reiterate the comments made above with respect to Miyanaga.

Even assuming *arguendo*, a proper motivation for combination, the fact that Cabral teaches that the width of **unthinned spacers** must be wide enough to avoid encroachment of the source/drain silicide contacts underneath the edges of the gate electrode e.g., from **200 Angstroms to 800 Angstroms** does not further help Examiner in establishing a *prima facie* case of obviousness.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)*.

4. Claim 3 stands rejected under 35 USC 103(a) as being unpatentable over Miyanaga, above, in view of Mikagi (US 6566254).

Applicants reiterate the comments made above with respect to Miyanaga.

Even assuming *arguendo*, a proper motivation for combination, the fact that Mikagi teaches a gate electrode of about 1000 Angstroms in width and that the trend of the semiconductor industry is to smaller dimensions does not further help Examiner in establishing a *prima facie* case of obviousness.

Examiner argues that Applicants have not shown the criticality of the gate length. While Examiner has not shown Applicants disclosed and claimed invention, Applicants nevertheless respond to this assertion by referring Examiner
to paragraph 0022:

"Referring to Figure 1E, in a **critical** aspect of the invention, a wet or dry etching process is then carried out to remove a portion of the nitride spacer 18B, to form a Slim (reduced width) oxide/nitride spacer width from W2 to W1. Advantageously, in the spacer thinning process a portion of the underlying SDE region e.g., 20A is exposed by the reduced width amount e.g., W3. For example, a maximum width W1 of the Slim spacers is preferably less than a width W2 of the

SDE doped regions e.g., 20A measured to an edge of the S/D doped region 22A. **It will be appreciated that the desired reduction in width of the nitride spacer portion 18B will vary depending on the gate length and the oxide/nitride spacer width W2 present for the S/D implant process prior to thinning, a desired reduction in S/D resistance, and a desired increase in channel stress.** Preferably, however, the Slim width W1 of the oxide/nitride spacer 18A and 18B measured from the polysilicon or metal gate electrode sidewall 14, is reduced by greater than about 20 percent of W2 to achieve a desired electrical resistance decrease in S/D region e.g., 22A and SDE region e.g., 20A and/or an increase in channel stress in channel region e.g., 26. In an exemplary embodiment, for a CMOS gate structure having a gate length (L_G), of about 400 Angstroms and a pre-Slim spacer width W2 of about 650 Angstroms, the spacer is reduced to a width W1 of less than about 500 Angstroms, more preferably less than about 350 Angstroms."

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

5. Claims 4 and 5 stand rejected under 35 USC 103(a) as being unpatentable over Miyanaga, above, in view of Ito (US 6656853).

Applicants reiterate the comments made above with respect to Miyanaga.

Ito teaches the formation of a silicon nitride film with a selected tensile or compressive stress over a conventional gate structure with **conventional spacers** (see col 5, lines 11-13), and discloses the effect of the stressed dielectric layer on charge mobility which Applicants also refer to in the discussion of the problem presented in the prior art.

There is no apparent motivation for combining the teachings of Miyanaga and Ito. Nowhere does Miyanaga recognize or suggest any type of stress exerted on a channel region would improve the operation of his device or whether it would interfere with the operation of a punch through stopper with respect to particular source drain orientation; likewise, nowhere does Ito suggest or discuss the effects of forming a punch through stopper under the gate electrode or the effect that formation of a particular source drain orientation would have on a particular type of stress exerted on a channel region by the stressed dielectric layer, or the effect of the dimensions or orientation of the spacers with respect to the gate electrode. For example, it is likely that a stress on the channel region and would adversely affect the operation of the punch through

stopper of Miyanaga.

Even assuming *arguendo*, a proper motivation for combination, such combination does not produce Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)*.

6. Claims 22 and 23 stand rejected under 35 USC 103(a) as being unpatentable over Huang above, in view of Ito (US 6656853).

Applicants reiterate the comments made above with respect to Huang and Ito.

Huang discloses spacers that **have a top portion lower than the top portion of the gate electrode** and nowhere recognizes or suggests formation of a stressed dielectric layer over the gate structure not recognize the effect of the dimensions or shape of the spacers

on stress induced into a channel region.

Ito discloses **conventional spacers** and nowhere suggests or recognizes the effect of the dimensions or shape of the spacers in relation to the gate electrode on stress induced into a channel region.

Even assuming *arguendo*, a proper motivation for combination, such combination does not produce Applicants disclosed and claimed invention.

7. Claim 25 stands rejected under 35 USC 103(a) as being unpatentable over Huang above, in view of Mikagi.

Applicants reiterate the comments made above with respect to Huang and Mikagi.

8. Claim 26 and 27 stand rejected under 35 USC 103(a) as being unpatentable over Huang above, in view of Cabral.

Applicants reiterate the comments made above with respect to Huang and Cabral.

The multiplicity of cited references, alone or in combination, do not produce Applicants disclosed and claimed invention and therefore do not make out a *prima facie* case of anticipation or obviousness with respect to Applicants disclosed and claimed invention.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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